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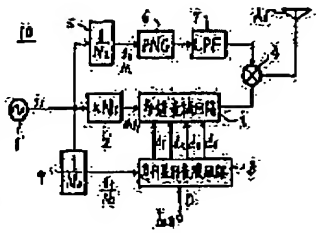
(54) SPREAD SPECTRUM MODULATOR AND/OR DEMODULATOR

(57)Abstract:

PURPOSE: To realize a high frequency use efficiency by constituting a modulator/ demodulator so that a carrier and a clock signal for spread code have synchronous relations and the carrier and a serial-parallel conversion output have synchronous relations.



CONSTITUTION: The reference signal having a frequency f1 is supplied to a multiplier 2 and frequency dividers 5 and 9 and is subjected to N2 and N3 frequency division and is supplied to a multilevel modulation circuit 3, a spread code generating circuit 6, and a serial-parallel conversion circuit 8. The circuit 8 subjects a series of information D from an input terminal In8 to serial-parallel conversion to obtain four signals d1 to d4 with a period f1/N3 and outputs them to the circuit 3. The circuit 3 subjects information signals d to d4 to multilevel modulation by the carrier having a frequency N1f1 from the multiplier and outputs the result to a multiplier 4. Meanwhile, the circuit 6 generates a spread code with the signal having a frequency f1/N2 from the frequency divider 5 as the clock signal and supplies it to the multiplier 4 through an LPF 7. Consequently, spread modulation of the multilevel modulation wave is performed by multiplication of the spread code in the multiplier 4, and the result is sent as an SS modulated wave.

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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] It is the frequency of a reference signal N1 The multiplier which carries out multiplying (N1 is the integer of arbitration), and obtains the subcarrier for a modulation, It is each about the frequency of the above-mentioned reference signal. 1/N2 It reaches. The 1st and 2nd counting-down circuit which carries out dividing to 1/N3 (N2 and N3 are the integer of arbitration), The diffusion sign generating circuit which generates a diffusion sign by making the output of this 1st counting-down circuit into a clock signal, The serial parallel-conversion circuit which carries out the serial parallel conversion of the input by making the output signal frequency of the 2nd counting-down circuit of the above into conversion timing, and is changed into two or more information signals, The spread-spectrum modulator which is equipped with the multi-level modulation circuit which carries out multi-level modulation of two or more information signals from this serial parallel-conversion circuit using the subcarrier from the above-mentioned multiplier, and the diffusion modulation means which carries out the diffusion modulation of the output of this multi-level modulation circuit using the above-mentioned diffusion sign at least, and sends out a spread-spectrum modulated wave.
[Claim 2] It is the spread-spectrum demodulator which receives a spread-spectrum modulated wave, gets over, and acquires the information on original, and is the frequency of a local oscillation signal N1 The multiplier which carries out multiplying, This N1 A frequency-conversion means to carry out the multiplication of the local oscillation signal by which multiplying was carried out to the above-mentioned spread-spectrum modulated wave, and to change this into an intermediate frequency, The diffusion sign generating circuit which generates a diffusion sign based on a clock signal, and the back-diffusion-of-electrons recovery means which carries out the back diffusion of electrons of this by carrying out the multiplication of the obtained diffusion sign to the output signal of the above-mentioned frequency-conversion means, The subcarrier regenerative circuit which reproduces a subcarrier based on the output of this back-diffusion-of-electrons recovery means, The multiple-value demodulator circuit which carries out the multiple-value recovery of the above-mentioned back-diffusion-of-electrons recovery output using the obtained subcarrier, and acquires two or more information signals, This subcarrier 1/N1 A reference signal playback means to acquire a playback reference signal equivalent to the reference signal at the time of a modulation by carrying out the multiplication of the signal and the above-mentioned local oscillation signal which carried out dividing, Acquired playback reference signal 1/N2 The counting-down circuit which carries out dividing and acquires the clock signal for diffusion sign generating, The synchronous detector which carries out change supply of the clock signal from this counting-down circuit in the above-mentioned diffusion sign generating circuit when the output signal of the above-mentioned back-diffusion-of-electrons recovery means is inputted and a correlating point is detected, Above-mentioned playback reference signal 1/N3 Spread-spectrum demodulator characterized by having at least the parallel-serial-conversion circuit which carries out the parallel serial conversion of two or more above-mentioned information signals by making into the signal for conversion timing the signal which carried out dividing.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a spread-spectrum modulation and/or a demodulator, and relates to the synchronous spread-spectrum modulation and/or synchronous demodulator which have improved frequency use effectiveness by adopting multi-level modulation, such as an amplitude phase modulation, as a primary modulation especially.
[0002]
[Background of the Invention] Although it was common sense that a spread-spectrum (it omits Following SS) communication link generally has low frequency use effectiveness, as for the frequency use effectiveness in a cellular-phone frequency band, the cellular phone of the CDMA (code division mulutiple access: code division multiple access) method which especially used SS in the U.S. is high rather by advance of the electronic technique of these days compared with the conventional wireless modulation recovery method. So, a U.S. CDMA method cellular phone attracts attention as a next-generation digital cellular phone, and even if it sees [standardizing etc. and] globally, the expansion to the public welfare field of SS technique has been increasing quickly.
[0003] There are some classes of the SS aiming at improvement in frequency use effectiveness. Two or more primary modulated waves which modulated one subcarrier with the approach of carrying out SS modulation after carrying out multi-level modulation of two or more information signals, and two or more information signals, and were obtained After carrying out a diffusion modulation using the diffusion sign which intersects perpendicularly with this and (which 90 degrees of phases differ), respectively, there is an approach of carrying out multiplex with the same frequency band or the approach of combining the former and the latter. In addition, as multi-level modulation, 16QAM (Quadrature Amplitude Modulation: quadrature amplitude modulation) which is generally one sort of an amplitude PE is used, and the primary modulation has adopted multi-level modulation like this 16QAM also in this invention equipment.
[0004]
[Description of the Prior Art] Conventional SS modulation and/or a conventional demodulator are explained with drawing 1 and drawing 2 . Drawing 1 is the outline block diagram of the conventional SS modulator (modulation transmitting section) 30 of the method which considers as a secondary modulation and performs SS modulation after carrying out multi-level modulation of two or more information signals as a primary modulation, and drawing 2 is the outline block diagram of the conventional SS demodulator (reception recovery section) 40 which gives SS recovery and a multiple-value recovery, and acquires the original information signal, after receiving the sending signal from the SS modulator 30.
[0005] In the usual transmitter, it is this SS modulator 30 and SS modem equipped with both SS demodulators 40, and they are antennas A1 and A2 in that case. Although combination of an oscillator 11 and 13 grades is also performed It is also theoretically possible to design both the equipments 30 and 40 according to an individual, and since actual communication is performed between transmitters different naturally, the SS modulator 30 and the SS demodulator 40 will be explained according to an individual, respectively.

[0006] It sets to the SS modulator 30 first, and they are input terminals In1, In2, In3, and In4. They are information signals d1, d2, d3, and d4, respectively. The multi-level modulation circuit 3 is supplied, and after performing multi-level modulation, such as a quadrature amplitude modulation, using the carrier signal from an oscillator 11 and acquiring a multi-level modulation signal, the diffusion modulation circuit 19 is supplied. On the other hand, a diffusion sign is generated in the diffusion sign generating circuit 6 based on the clock signal from an oscillator (source of a clock signal) 12, this is supplied to the diffusion modulation circuit 19, the diffusion modulation of the above-mentioned multi-level modulation signal is carried out further, and it is the antenna A1 for transmission. It sends out as an SS modulated wave.
[0007] Next, the configuration and actuation of the SS demodulator 40 are explained. After supplying first SS modulated wave which received with the receiving antenna A2 to a frequency changing circuit 61 and performing frequency conversion by multiplication with the signal from a local oscillator 13 here, the back-diffusion-of-electrons demodulator circuit 62 and the SS synchronous holding circuit 63 are supplied. As an example of the SS synchronous holding circuit 63, there are a DLL (delay locked loop) mold synchronous holding circuit, a TDL (tau dither loop) mold synchronous holding circuit, etc.
[0008] In order to establish SS synchronization in SS recovery Like common knowledge, the output signal of the back-diffusion-of-electrons demodulator circuit 62 is supplied to SS synchronous detection / synchronous prehension circuit 64. SS synchronous prehension is first performed by detecting the peak level in the synchronous detection stage in a circuit 64. SS synchronization is established by switching the circuit of the SS synchronous holding circuit 63 interior to synchronous maintenance from synchronous detection with SS synchronous prehension signal, and performing synchronous maintenance actuation by the feedback loop of the SS synchronous holding circuit 63.
[0009] After an appropriate time, a back-diffusion-of-electrons recovery is normally performed using the diffusion sign generated in the diffusion sign generating circuit in the SS synchronous holding circuit 63 (not shown). A back-diffusion-of-electrons recovery output is supplied also to the subcarrier regenerative circuit 37 and the multiple-value demodulator circuit 42. Since a 16QAM recovery is given as a multiple-value recovery, playback of the subcarrier for performing a synchronous recovery is needed. Then, a back-diffusion-of-electrons recovery signal is outputted also to the subcarrier regenerative circuit 37, a subcarrier is reproduced by predetermined signal processing, and the multiple-value demodulator circuit 42 is supplied. A multiple-value recovery (primary recovery) is performed by this in the multiple-value demodulator circuit 42, and they are the recovery information signals d1, d2, d3, and d4, more nearly respectively than each output terminals Out1-Out4. It has obtained. In addition, generally as a subcarrier regenerative circuit 37, the Costas loop formation (Costas loop) is used like common knowledge.
[0010] Each synchronous loop formation for recovery actuation is constituted from conventional equipment 40 of this configuration by the SS synchronous holding circuit 63, SS synchronous detection / synchronous prehension circuit 64, and the subcarrier regenerative-circuit 37 grade so that more clearly than drawing 2 . SS synchronous detection activity (actuation) and SS synchronous prehension activity are done first in SS synchronous detection / synchronous prehension circuit 64. Next, as soon as it moves to SS synchronous maintenance activity by the SS synchronous holding circuit 63 and SS recovery activity [in the back-diffusion-of-electrons demodulator circuit 62] finishes The subcarrier playback activity for the synchronous recovery in a multiple-value recovery is done in the subcarrier regenerative circuit 37, and actuation of the demodulator 40 whole starts by using a playback subcarrier finally and starting a synchronous recovery in the multiple-value demodulator circuit 42.
[0011] Here, the concrete configuration of the multi-level modulation circuit 3 of a 16QAM method and the multiple-value demodulator circuit 42, the principle of operation of 16QAM, etc. are briefly explained with drawing 3 and drawing 4 . drawing 3 R> 3 and drawing 4 are the concrete block diagrams of the multi-level modulation circuit 3 used conventionally and the multiple-value demodulator circuit 42, and can be set in the multi-level modulation circuit 3 — each — input terminal In1 -In4 and the SS modulator 30 which showed each output terminals

Out1-Out4 in the multiple-value demodulator circuit 42 to said drawing 1 and drawing 2, respectively — each — input terminal In1 -In4 And it is in common (the same), respectively with each output terminals Out1-Out4 of the SS demodulator 40.
[0012] As the multi-level modulation circuit 3 is first shown in drawing 3, it is an input terminal In5. It minds, a subcarrier is directly supplied to multipliers 53 and 55 from the oscillator 11 of said drawing 1, and it is a phase in a phase-shifting circuit 52 to multipliers 54 and 56 pi/2 It supplies, after shifting. on the other hand — input terminals In1, In2, In3, and In4 from — information signals d1, d2, d3, and d4 (data with which all consist of binary [of 0 or 1]) are supplied to multipliers 53-56, respectively, and the phase modulation by multiplication with the above-mentioned subcarrier or the subcarrier by which pi / 2 phase shifts were carried out is performed. Therefore, if the output of a multiplier 53 and the output of a multiplier 54 are added with an adder 57, the addition output will serve as a 4 phase PSK signal, and it is this phi 1 (t) It will express. Similarly, the output of a multiplier 55 and a multiplier 56 is added with an adder 58, and it is the 4 phase PSK signal phi 2. (t) It obtains.
[0013] Furthermore, 4 phase PSK signal phi 2 (t) It is with an attenuator 51 about a transmission level. One half After lowering, it is the 4 phase PSK signal phi 1. (t) Although the addition output will serve as a 16QAM signal with which amplitude modulation was also performed and it will be outputted from a terminal Out5 if it adds with an adder 59 The tooth-space diagram (signal point arrangement) serves as bit allocation (tooth-space diagram) of **** 16QAM shown in drawing 5 as an example [refer to Ohm-Sha issue "the foundation of a digital strange demodulator circuit"].

[0014] Next, the principle of operation of the multiple-value demodulator circuit 42 is explained with drawing 4. The 16QAM signal from the back-diffusion-of-electrons demodulator circuit 62 of said drawing 2 is an input terminal In6. It minds and the multipliers 74 and 75 for a synchronous recovery are supplied. On the other hand, it is an input terminal In7. It minds, a subcarrier is directly supplied to a multiplier 74 from the subcarrier regenerative circuit 37 of drawing 2, and it is a phase in a phase-shifting circuit 73 in a multiplier 75 pi/2 It supplies, after shifting. therefore — since the subcarrier for this synchronous recovery has been obtained by extracting the subcarrier contained in a 16QAM signal from the back-diffusion-of-electrons demodulator circuit 62 as shown in drawing 2 although the synchronous recovery by multiplication with each subcarrier is performed in multipliers 74 and 75, respectively — the frequency — input terminal In6 from — naturally it is the same as that of the frequency of the subcarrier contained in a 16QAM signal.
[0015] Therefore, from a multiplier 74, it sets in said multi-level modulation circuit 3, and is pi/2. Information signal d1 to which multiplication with the subcarrier by which a phase shift is not carried out was given Information signal d3 It is outputted through LPF76. Similarly, from a multiplier 75, it sets in the multi-level modulation circuit 3, and is pi/2. Information signal d2 by which multiplication was carried out to the subcarrier by which the phase shift was carried out Information signal d4 It is outputted through LPF77. Information signal d3 which had the transmission level reduced by half with the attenuator 51 in said multi-level modulation circuit 3 among each output of these LPF 76 and 77 Information signal d4 Since it is eliminated in the level discrimination decision circuits 78 and 79, respectively, from output terminals Out1 and Out2, it is an information signal d1, respectively. And information signal d2 It is outputted. Therefore, it is the information signal d3 which is having level reduced by half from the subtraction circuits 80 and 81. Information signal d4 It is outputted, respectively, and transmission gain is returned to the original level with the amplifiers 82 and 83 of 2, and is outputted from output terminals Out3 and Out4, respectively.
[0016]
[Problem(s) to be Solved by the Invention] In the conventional spread-spectrum modulation and/or conventional demodulator which combined this multi-level modulation recovery and said SS modulation recovery, as already explained in SS synchronous maintenance, the DLL mold synchronous holding circuit or the TDL mold synchronous holding circuit is used. Therefore, the problem of complication of the circuitry especially in the SS demodulator 40 and increase-izing is not avoided, but comparatively long SS synchronous establishment time amount decided by

the response time of the loop formation in the SS synchronous holding circuit 63 and the operating time in SS synchronous detection / synchronous prehension circuit 64, the response time of the loop formation in the subsequent subcarrier regenerative circuit 37, etc. are added further, and the problem which will require time amount too much before the SS demodulator 40 whole results in the recovery operating state of a stationary exists.
[0017] So that it may guess from drawing 5 by the multi-level modulation method Moreover, since the eye of an eye pattern is fundamentally small, In order to require the cure against a jitter very severely and to turn to only the specific application of the good transmission system of C/N, it sets especially about combination (use in a primary modulation) with SS. There was a theoretic fault of being easy to produce an error to the information on data etc. according to generating of the jitter component by the mutual intervention between the various frequency components which contain a diffusion sign in equipment.
[0018]
[Means for Solving the Problem] This invention offers the spread-spectrum modulation and/or demodulator of the following configurations, in order to solve the above-mentioned technical problem.
[0019] First, a spread-spectrum modulator is the frequency of a reference signal N1 The multiplier which carries out multiplying and obtains the subcarrier for a modulation, It is each about the frequency of a reference signal. 1/N2 It reaches. The 1st and 2nd counting-down circuit which carries out dividing to 1/N3 (N1, and N2 and N3 are the integer of arbitration), The diffusion sign generating circuit which generates a diffusion sign by making the output of the 1st counting-down circuit into a clock signal, The serial parallel-conversion circuit which carries out the serial parallel conversion of the input by making the output signal frequency of the 2nd counting-down circuit into conversion timing, and is changed into two or more information signals, It has the multi-level modulation circuit which carries out multi-level modulation of two or more information signals from this serial parallel-conversion circuit using the subcarrier from the above-mentioned multiplier, the diffusion modulation means which carries out the diffusion modulation of the multi-level modulation circuit output using a diffusion sign.
[0020] Moreover, a spread-spectrum demodulator is the frequency of a local oscillation signal N1 The multiplier which carries out multiplying, N1 A frequency-conversion means to carry out the multiplication of the local oscillation signal by which multiplying was carried out to a spread-spectrum modulated wave, and to change this into an intermediate frequency, The diffusion sign generating circuit which generates a diffusion sign based on a clock signal, and the back-diffusion-of-electrons recovery means which carries out the back diffusion of electrons of this by carrying out the multiplication of the obtained diffusion sign to the output signal of the above-mentioned frequency-conversion means, The subcarrier regenerative circuit which reproduces a subcarrier based on the output of this back-diffusion-of-electrons recovery means, The multiple-value demodulator circuit which carries out the multiple-value recovery of the above-mentioned back-diffusion-of-electrons recovery output using the obtained subcarrier, and acquires two or more information signals, It is the obtained subcarrier 1/N1 A reference signal playback means to acquire a playback reference signal equivalent to the reference signal at the time of a modulation by carrying out the multiplication of the signal and the above-mentioned local oscillation signal which carried out dividing, Acquired playback reference signal 1/N2 The counting-down circuit which carries out dividing and acquires the clock signal for diffusion sign generating, The synchronous detector which carries out change supply of the clock signal from a counting-down circuit in the above-mentioned diffusion sign generating circuit when the output signal of the above-mentioned back-diffusion-of-electrons recovery means is inputted and a correlating point is detected, Above-mentioned playback reference signal 1/N3 It has the parallel-serial-conversion circuit which carries out the parallel serial conversion of two or more above-mentioned information signals by making into the signal for conversion timing the signal which carried out dividing.
[0021]
[Example] SS modulation and/or the demodulator of this invention are ** explained with reference to drawing 6 etc. Drawing 6 is the block diagram showing one example of the SS

modulator 10 of this invention. It sets to this drawing and, for a reference signal generator (oscillator) and 2, the number of multiplying is [1] N1. Frequency multiplier [it is only described as a "multiplier" below], the multiplier for a diffusion modulation in 4, and 5 and 9 — the number of dividing — respectively — N2 and N3 (each of N1, N2, and N3 is the integer of arbitration) — a counting-down circuit — The same sign is given to the same component as equipment 30 conventionally which 7 is LPF, and 8 is a serial juxtaposition (S/P) conversion circuit, in addition was shown in drawing 1 , and the detailed explanation is omitted. In addition, the concrete configuration of the multi-level modulation circuit 3 is as having been shown in drawing 3 .

[0022] Next, concrete actuation of the SS modulator 10 is explained with reference to drawing 6 . Frequency f1 outputted from an oscillator 1 A multiplier 2 and counting-down circuits 5 and 9 are supplied, and a reference signal is N1, respectively. Multiplying and N2 Dividing and N3 After dividing is carried out, the multi-level modulation circuit 3, the diffusion sign generating circuit 6, and the serial juxtaposition (SHIRIPARA) conversion circuit 8 are supplied, respectively.

[0023] thereby — the serial parallel-conversion circuit 8 — setting — input terminal In8 from — a series of information Df1 / N3 a period (conversion timing) — four information signals d1, d2, d3, and d4 the serial parallel conversion is carried out — [— each information — transmission speed [ ] —] which falls to one fourth. Or four information signal d1 -d4 supplied serially It changes into four juxtaposition-signals and outputs to the multi-level modulation circuit 3. And in the multi-level modulation circuit 3, it is the frequency N one f1 from a multiplier 2. It is information signal d1 -d4 by the subcarrier. Multi-level modulation (for example, 16QAM) is carried out, and it is outputting to the multiplier 4.

[0024] On the other hand, in the diffusion sign generating circuit 6, it is f1 from a counting-down circuit 5 / N2. The diffusion sign for a diffusion modulation is generated by making the signal of a frequency into a clock signal, and the multiplier 4 is supplied through LPF7. Therefore, in a multiplier 4, the diffusion modulation of the multi-level modulation wave by multiplication with a diffusion sign is performed, and it is the transmitting antenna A1. It is sent out as an SS modulated wave. In addition, LPF7 may remove components other than the main lobe of a diffusion sign, and there may not not necessarily be. By the way, the period of a diffusion sign (clock signal), the subcarrier for multi-level modulation, and a serial parallel conversion has taken the synchronization so that clearly from the above explanation.

[0025] Next, the SS demodulator 20 is explained with drawing 7 . As shown in this drawing, the SS demodulator 20 of this invention is two or more BPF (band pass filter) 22, 27, and 31, the 46; various amplifier 23, and the 41; mixers (multiplier) 24, 28, and 39 ;P NG (diffusion coder)29, the AGC amplifier 32, counting-down circuits 36, 38, and 44; it has the synchronous detector 33 and parallel-serial (P/S) conversion circuit 43 grade, and these are connected like illustration and it is constituted. In addition, the same sign is given to the same component as equipment 2 conventionally which was shown in drawing 2 in this drawing 7 , and that detailed explanation is omitted. Moreover, the concrete configuration of the multiple-value demodulator circuit 42 is as having been shown in drawing 4 .

[0026] Receiving antenna A2 SS modulated wave which received is supplied to a mixer 24 through BPF22 and the RF amplifier 23. On the other hand, the local oscillation signal outputted from a local oscillator 25 is a frequency by the multiplier 26 N1 Multiplying is carried out, it considers as a multiplying local oscillation signal, and the mixer 24 is supplied. Therefore, frequency conversion of the SS modulated wave is carried out to an intermediate frequency by the mixer 24, and a multiplier 28 is supplied through BPF27.

[0027] On the other hand from the oscillator 35 for synchronous prehension, the signal for synchronous prehension with the frequency near the clock signal frequency for diffusion signs of normal is outputted, and this oscillation signal is supplied before SS synchronous establishment to PNG29 through Switch Sw. Therefore, since the diffusion sign for synchronous prehension is outputted from PNG29 and a multiplier 28 is supplied through LPF21, the output of a multiplier 28 turns into a correlation output for SS synchronous prehension. Short SS synchronous point (correlating point) and a comparatively prolonged asynchronous period exist in this correlation output like common knowledge repeatedly in time, and this correlation output is supplied to the multiple-value demodulator circuit 42, the subcarrier regenerative circuit 37, and the

synchronous detector 33 through BPF31 and the AGC (automatic gain control) amplifier 32.

[0028] In the decorrelational period of the above-mentioned correlation output, since SS synchronization is not established, a playback subcarrier with many jitters is outputted from the subcarrier regenerative circuit 37, but if it results in a correlating point, the jitter in a playback subcarrier will serve as the minimum. At the correlating point of this short period of time, the playback subcarrier which does not almost have a jitter is N1 dividing. A counting-down circuit 38, a multiplier 39, BPF46, an amplifier 41, and N2 dividing Switch Sw is supplied through a counting-down circuit 36. Since the local oscillation signal from a local oscillator 25 is also supplied to the multiplier 39, it is 1/N1 here. Multiplication with the correlation output by which dividing was carried out is performed. Therefore, from a multiplier 39, two kinds of signals which have the sum of the frequency of both input signals and the frequency of a difference, respectively are outputted. It is the frequency f1 of the reference signal which uses the frequency with said SS modulator 10 like the after-mentioned although only a signal component with a peace (a difference is sufficient) frequency is made to transmit by this example among them BPF46. It becomes the very thing.

[0029] That is, a counting-down circuit 36 is supplied through amplifier 41, and the reference signal which a reference signal playback means is formed and was reproduced by the multiplier 39 and BPF46 here is 1/N2 here. Since dividing is carried out, as for the output, the SS modulator 10 serves as the same a clock signal for diffusion sign generating. On the other hand, if the correlation output supplied to the synchronous detector 33 serves as a correlating point, by detecting for example, threshold level, the synchronous detector 33 will detect it and will output a control signal to Switch Sw. Then, since Switch Sw switches connection to a counting-down circuit 36 side from an oscillator 35, the above-mentioned playback clock signal from a counting-down circuit 36 is supplied to the diffusion coder 29, a diffusion sign equivalent to the diffusion sign in the SS modulator 10 comes to be generated, and SS synchronization is established.

[0030] Moreover, since the jitter of a playback subcarrier serves as the minimum, the recovery actuation in the multiple-value demodulator circuit 42 will also start to SS synchronous establishment and coincidence in an instant, and a multi-level modulation signal restores to it to them in this multiple-value demodulator circuit 42 by the circuitry and the principle of operation which were shown at said drawing 4 , and it is information signal d1 -d4. It is outputted to the parallel-serial-conversion circuit 43 at parallel.

[0031] On the other hand, for the playback reference signal from amplifier 41, the number of dividing is N3. Since the parallel-serial-conversion circuit 43 is supplied as a clock signal through a counting-down circuit 44 [the counting-down circuit 9 of the SS modulator 10, and this function], it is information signal d1 -d4 by parallel-serial (PARASHIRI) conversion. It is changed into the information D on a radical, and is outputted from an output terminal Out6.

[0032] Here, in the SS demodulator 20, drawing 6 drawing 7 is combined, the process in which a playback reference signal is reproduced is referred to, and it explains to ** et al and a detail. the reference signal frequency from said oscillator 1 — like the above — f1 it is — several multiplying of multipliers 2 and 26 — N1 the carrier frequency which will be supplied to the multi-level modulation circuit 3 if 9 — 9f1 It becomes. Moreover, it is the local oscillation signal frequency from the oscillator 25 in the SS demodulator 20 f2 When it carries out, the multiplying local oscillation signal frequency from a multiplier 26 is 2 9f. It becomes, and the frequency will be set to 9 (f1-f2) if the signal which has the frequency component of a difference among [BPF27] the multiplication outputs from a mixer 24 is made to transmit.

[0033] Therefore, the frequency of the playback subcarrier through BPF31 and amplifier 32 of the subcarrier regenerative circuit 37 is also 9 (f1-f2). On the other hand, for the frequency (fundamental frequency) of the dividing output signal of a counting-down circuit 38, the frequency of the signal which removes a frequency component unnecessary among the multiplication outputs from a multiplier 39 at BPF46, and is acquired since it is (f1-f2) is (f1-f2) +f2 =f1. Since it becomes, it is a frequency f1 from BPF46. It means that the reference signal was reproduced.

[0034] In addition, in this invention, the build up time of the actuation in the SS demodulator 20

is computed as follows. namely, the clock signal frequency for diffusion signs — f1 / N2 it is — if f3 and diffusion code length are set to L for the frequency of the signal for synchronous prehension from an oscillator 1, the synchronous prehension time amount T will become settled in a degree type.

[0035]

T<=L {f1/N2-f3} -1 ..... (1) They are code length L= 31 and f1/N2-f3 =1kHz there. It is T<=31msec if it carries out. It becomes, namely, they are 31msec(s). SS synchronization will be established in a short time called the following. On the other hand, for the subcarrier regenerative circuit 37, since it has started before SS synchronization is established, the sum total of build up time is these 31msec(s). It will fit in less than.

[0036] In the above explanation, although multi-level modulation was made into 16QAM, it is theoretically possible not only this but to make it 64QAM etc., and, naturally the serial parallel conversion of the information D is carried out to eight information signals (d1 -d8) in that case.

[0037]

[Effect of the Invention] Like the above statement, according to SS modulation and/or the demodulator of this invention, a subcarrier, the clock signal for diffusion signs, and a subcarrier and information (serial parallel-conversion output) are constituted so that it may have synchronous relation. Therefore, since a problem is lost, therefore the combination use of equipment of a multi-level modulation recovery and SS modulation recovery becomes [in / since the interference problem in equipment can be reduced sharply / application of multi-level modulation/recovery] possible, it is realizable as equipment with high frequency use effectiveness.

[0038] Moreover, build up time of actuation of a receiving demodulator Since it becomes settled uniquely as shown in (1) type, equipment with the early rate of rise is realizable. And since SS synchronous supporting structure which was the requirements for a configuration more indispensable than before became unnecessary, circuitry is simplified and the overall cost of equipment becomes cheap, it has the features which were excellent in many — broad application is attained.

[Translation done.]

TECHNICAL FIELD

[Industrial Application] This invention relates to a spread-spectrum modulation and/or a demodulator, and relates to the synchronous spread-spectrum modulation and/or synchronous demodulator which have improved frequency use effectiveness by adopting multi-level modulation, such as an amplitude phase modulation, as a primary modulation especially.

[0002]

[Background of the Invention] Although it was common sense that a spread-spectrum (it omits Following SS) communication link generally has low frequency use effectiveness, as for the frequency use effectiveness in a cellular-phone frequency band, the cellular phone of the CDMA (code division multiple access: code division multiple access) method which especially used SS in the U.S. is high rather by advance of the electronic technique of these days compared with the conventional wireless modulation recovery method. So, a U.S. CDMA method cellular phone attracts attention as a next-generation digital cellular phone, and even if it sees [standardizing etc. and] globally, the expansion to the public welfare field of SS technique has been increasing quickly.

[0003] There are some classes of the SS aiming at improvement in frequency use effectiveness. Two or more primary modulated waves which modulated one subcarrier with the approach of carrying out SS modulation after carrying out multi-level modulation of two or more information signals, and two or more information signals, and were obtained After carrying out a diffusion modulation using the diffusion sign which intersects perpendicularly with this and (which 90 degrees of phases differ), respectively, there is an approach of carrying out multiplex with the same frequency band or the approach of combining the former and the latter. In addition, as multi-level modulation, 16QAM (Quadrature Amplitude Modulation: quadrature amplitude modulation) which is generally one sort of an amplitude PE is used, and the primary modulation has adopted multi-level modulation like this 16QAM also in this invention equipment.

[Translation done.]

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3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] Conventional SS modulation and/or a conventional demodulator are explained with drawing 1 and drawing 2 . Drawing 1 is the outline block diagram of the conventional SS modulator (modulation transmitting section) 30 of the method which considers as a secondary modulation and performs SS modulation after carrying out multi-level modulation of two or more information signals as a primary modulation, and drawing 2 is the outline block diagram of the conventional SS demodulator (reception recovery section) 40 which gives SS recovery and a multiple-value recovery, and acquires the original information signal, after receiving the sending signal from the SS modulator 30.
[0005] In the usual transmitter, it is this SS modulator 30 and SS modem equipped with both SS demodulators 40, and they are antennas A1 and A2 in that case. Although combination of an oscillator 11 and 13 grades is also performed It is also theoretically possible to design both the equipments 30 and 40 according to an individual, and since actual communication is performed between transmitters different naturally, the SS modulator 30 and the SS demodulator 40 will be explained according to an individual, respectively.
[0006] It sets to the SS modulator 30 first, and they are input terminals In1, In2, In3, and In4. They are information signals d1, d2, d3, and d4, respectively. The multi-level modulation circuit 3 is supplied, and after performing multi-level modulation, such as a quadrature amplitude modulation, using the carrier signal from an oscillator 11 and acquiring a multi-level modulation signal, the diffusion modulation circuit 19 is supplied. On the other hand, a diffusion sign is generated in the diffusion sign generating circuit 6 based on the clock signal from an oscillator (source of a clock signal) 12, this is supplied to the diffusion modulation circuit 19, the diffusion modulation of the above-mentioned multi-level modulation signal is carried out further, and it is the antenna A1 for transmission. It sends out as an SS modulated wave.
[0007] Next, the configuration and actuation of the SS demodulator 40 are explained. After supplying first SS modulated wave which received with the receiving antenna A2 to a frequency changing circuit 61 and performing frequency conversion by multiplication with the signal from a local oscillator 13 here, the back-diffusion-of-electrons demodulator circuit 62 and the SS synchronous holding circuit 63 are supplied. As an example of the SS synchronous holding circuit 63, there are a DLL (delay locked loop) mold synchronous holding circuit, a TDL (tau dither loop) mold synchronous holding circuit, etc.
[0008] In order to establish SS synchronization in SS recovery Like common knowledge, the output signal of the back-diffusion-of-electrons demodulator circuit 62 is supplied to SS synchronous detection / synchronous prehension circuit 64. SS synchronous prehension is first performed by detecting the peak level in the synchronous detection stage in a circuit 64. SS synchronization is established by switching the circuit of the SS synchronous holding circuit 63 interior to synchronous maintenance from synchronous detection with SS synchronous prehension signal, and performing synchronous maintenance actuation by the feedback loop of the SS synchronous holding circuit 63.
[0009] After an appropriate time, a back-diffusion-of-electrons recovery is normally performed using the diffusion sign generated in the diffusion sign generating circuit in the SS synchronous holding circuit 63 (not shown). A back-diffusion-of-electrons recovery output is supplied also to

the subcarrier regenerative circuit 37 and the multiple-value demodulator circuit 42. Since a 16QAM recovery is given as a multiple-value recovery, playback of the subcarrier for performing a synchronous recovery is needed. Then, a back-diffusion-of-electrons recovery signal is outputted also to the subcarrier regenerative circuit 37, a subcarrier is reproduced by predetermined signal processing, and the multiple-value demodulator circuit 42 is supplied. A multiple-value recovery (primary recovery) is performed by this in the multiple-value demodulator circuit 42, and they are the recovery information signals d1, d2, d3, and d4, more nearly respectively than each output terminals Out1-Out4. It has obtained. In addition, generally as a subcarrier regenerative circuit 37, the Costas loop formation (Costas loop) is used like common knowledge.
[0010] Each synchronous loop formation for recovery actuation is constituted from conventional equipment 40 of this configuration by the SS synchronous holding circuit 63, SS synchronous detection / synchronous prehension circuit 64, and the subcarrier regenerative-circuit 37 grade so that more clearly than drawing 2 . SS synchronous detection activity (actuation) and SS synchronous prehension activity are done first in SS synchronous detection / synchronous prehension circuit 64. Next, as soon as it moves to SS synchronous maintenance activity by the SS synchronous holding circuit 63 and SS recovery activity [in the back-diffusion-of-electrons demodulator circuit 62] finishes The subcarrier playback activity for the synchronous recovery in a multiple-value recovery is done in the subcarrier regenerative circuit 37, and actuation of the demodulator 40 whole starts by using a playback subcarrier finally and starting a synchronous recovery in the multiple-value demodulator circuit 42.
[0011] Here, the concrete configuration of the multi-level modulation circuit 3 of a 16QAM method and the multiple-value demodulator circuit 42, the principle of operation of 16QAM, etc. are briefly explained with drawing 3 and drawing 4 . drawing 3 R> 3 and drawing 4 are the concrete block diagrams of the multi-level modulation circuit 3 used conventionally and the multiple-value demodulator circuit 42, and can be set in the multi-level modulation circuit 3 — each — input terminal In1 -In4 and the SS modulator 30 which showed each output terminals Out1-Out4 in the multiple-value demodulator circuit 42 to said drawing 1 and drawing 2 , respectively — each — input terminal In1 -In4 And it is in common (the same), respectively with each output terminals Out1-Out4 of the SS demodulator 40.
[0012] As the multi-level modulation circuit 3 is first shown in drawing 3 , it is an input terminal In5. It minds, a subcarrier is directly supplied to multipliers 53 and 55 from the oscillator 11 of said drawing 1 , and it is a phase in a phase-shifting circuit 52 to multipliers 54 and 56 pi/2 It supplies, after shifting, on the other hand — input terminals In1, In2, In3, and In4 from — information signals d1, d2, d3, and d4 (data with which all consist of binary [of 0 or 1]) are supplied to multipliers 53-56, respectively, and the phase modulation by multiplication with the above-mentioned subcarrier or the subcarrier by which pi / 2 phase shifts were carried out is performed. Therefore, if the output of a multiplier 53 and the output of a multiplier 54 are added with an adder 57, the addition output will serve as a 4 phase PSK signal, and it is this phi 1 (t) It will express. Similarly, the output of a multiplier 55 and a multiplier 56 is added with an adder 58, and it is the 4 phase PSK signal phi 2. (t) It obtains.
[0013] Furthermore, 4 phase PSK signal phi 2 (t) It is with an attenuator 51 about a transmission level. One half After lowering, it is the 4 phase PSK signal phi 1. (t) Although the addition output will serve as a 16QAM signal with which amplitude modulation was also performed and it will be outputted from a terminal Out5 if it adds with an adder 59 The tooth-space diagram (signal point arrangement) serves as bit allocation (tooth-space diagram) of **** 16QAM shown in drawing 5 as an example [refer to Ohm-Sha issue "the foundation of a digital strange demodulator circuit"].

[0014] Next, the principle of operation of the multiple-value demodulator circuit 42 is explained with drawing 4 . The 16QAM signal from the back-diffusion-of-electrons demodulator circuit 62 of said drawing 2 is an input terminal In6. It minds and the multipliers 74 and 75 for a synchronous recovery are supplied. On the other hand, it is an input terminal In7. It minds, a subcarrier is directly supplied to a multiplier 74 from the subcarrier regenerative circuit 37 of drawing 2 , and it is a phase in a phase-shifting circuit 73 in a multiplier 75 pi/2 It supplies, after

shifting. therefore — since the subcarrier for this synchronous recovery has been obtained by extracting the subcarrier contained in a 16QAM signal from the back-diffusion-of-electrons demodulator circuit 62 as shown in drawing 2 although the synchronous recovery by multiplication with each subcarrier is performed in multipliers 74 and 75, respectively — the frequency — input terminal In6 from — naturally it is the same as that of the frequency of the subcarrier contained in a 16QAM signal.

[0015] Therefore, from a multiplier 74, it sets in said multi-level modulation circuit 3, and is pi/2. Information signal d1 to which multiplication with the subcarrier by which a phase shift is not carried out was given Information signal d3 It is outputted through LPF76. Similarly, from a multiplier 75, it sets in the multi-level modulation circuit 3, and is pi/2. Information signal d2 by which multiplication was carried out to the subcarrier by which the phase shift was carried out Information signal d4 It is outputted through LPF77. Information signal d3 which had the transmission level reduced by half with the attenuator 51 in said multi-level modulation circuit 3 among each output of these LPF 76 and 77 Information signal d4 Since it is eliminated in the level discrimination decision circuits 78 and 79, respectively, from output terminals Out1 and Out2, it is an information signal d1, respectively. And information signal d2 It is outputted. Therefore, it is the information signal d3 which is having level reduced by half from the subtraction circuits 80 and 81. Information signal d4 It is outputted, respectively, and transmission gain is returned to the original level with the amplifiers 82 and 83 of 2, and is outputted from output terminals Out3 and Out4, respectively.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] Like the above statement, according to SS modulation and/or the demodulator of this invention, a subcarrier, the clock signal for diffusion signs, and a subcarrier and information (serial parallel-conversion output) are constituted so that it may have synchronous relation. Therefore, since a problem is lost, therefore the combination use of equipment of a multi-level modulation recovery and SS modulation recovery becomes [in / since the interference problem in equipment can be reduced sharply / application of multi-level modulation/recovery] possible, it is realizable as equipment with high frequency use effectiveness.

[0038] Moreover, build up time of actuation of a receiving demodulator Since it becomes settled uniquely as shown in (1) type, equipment with the early rate of rise is realizable. And since SS synchronous supporting structure which was the requirements for a configuration more indispensable than before became unnecessary, circuitry is simplified and the overall cost of equipment becomes cheap, it has the features which were excellent in many — broad application is attained.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the conventional spread-spectrum modulation and/or conventional demodulator which combined this multi-level modulation recovery and said SS modulation recovery, as already explained in SS synchronous maintenance, the DLL mold synchronous holding circuit or the TDL mold synchronous holding circuit is used. Therefore, the problem of complication of the circuitry especially in the SS demodulator 40 and increase-izing is not avoided, but comparatively long SS synchronous establishment time amount decided by the response time of the loop formation in the SS synchronous holding circuit 63 and the operating time in SS synchronous detection / synchronous prehension circuit 64, the response time of the loop formation in the subsequent subcarrier regenerative circuit 37, etc. are added further, and the problem which will require time amount too much before the SS demodulator 40 whole results in the recovery operating state of a stationary exists.
[0017] So that it may guess from drawing 5 by the multi-level modulation method Moreover, since the eye of an eye pattern is fundamentally small, In order to require the cure against a jitter very severely and to turn to only the specific application of the good transmission system of C/N, it sets especially about combination (use in a primary modulation) with SS. There was a theoretic fault of being easy to produce an error to the information on data etc. according to generating of the jitter component by the mutual intervention between the various frequency components which contain a diffusion sign in equipment.

[Translation done.]

MEANS

[Means for Solving the Problem] This invention offers the spread-spectrum modulation and/or demodulator of the following configurations, in order to solve the above-mentioned technical problem.
[0019] First, a spread-spectrum modulator is the frequency of a reference signal N1 The multiplier which carries out multiplying and obtains the subcarrier for a modulation, It is each about the frequency of a reference signal. 1/N2 It reaches. The 1st and 2nd counting-down circuit which carries out dividing to 1/N3 (N1, and N2 and N3 are the integer of arbitration), The diffusion sign generating circuit which generates a diffusion sign by making the output of the 1st counting-down circuit into a clock signal, The serial parallel-conversion circuit which carries out the serial parallel conversion of the input by making the output signal frequency of the 2nd counting-down circuit into conversion timing, and is changed into two or more information signals, It has the multi-level modulation circuit which carries out multi-level modulation of two or more information signals from this serial parallel-conversion circuit using the subcarrier from the above-mentioned multiplier, the diffusion modulation means which carries out the diffusion modulation of the multi-level modulation circuit output using a diffusion sign.
[0020] Moreover, a spread-spectrum demodulator is the frequency of a local oscillation signal N1 The multiplier which carries out multiplying, N1 A frequency-conversion means to carry out the multiplication of the local oscillation signal by which multiplying was carried out to a spread-spectrum modulated wave, and to change this into an intermediate frequency, The diffusion sign generating circuit which generates a diffusion sign based on a clock signal, and the back-diffusion-of-electrons recovery means which carries out the back diffusion of electrons of this by carrying out the multiplication of the obtained diffusion sign to the output signal of the above-mentioned frequency-conversion means, The subcarrier regenerative circuit which reproduces a subcarrier based on the output of this back-diffusion-of-electrons recovery means, The multiple-value demodulator circuit which carries out the multiple-value recovery of the above-mentioned back-diffusion-of-electrons recovery output using the obtained subcarrier, and acquires two or more information signals, It is the obtained subcarrier 1/N1 A reference signal playback means to acquire a playback reference signal equivalent to the reference signal at the time of a modulation by carrying out the multiplication of the signal and the above-mentioned local oscillation signal which carried out dividing, Acquired playback reference signal 1/N2 The counting-down circuit which carries out dividing and acquires the clock signal for diffusion sign generating, The synchronous detector which carries out change supply of the clock signal from a counting-down circuit in the above-mentioned diffusion sign generating circuit when the output signal of the above-mentioned back-diffusion-of-electrons recovery means is inputted and a correlating point is detected, Above-mentioned playback reference signal 1/N3 It has the parallel-serial-conversion circuit which carries out the parallel serial conversion of two or more above-mentioned information signals by making into the signal for conversion timing the signal which carried out dividing.

[Translation done.]

EXAMPLE

[Example] SS modulation and/or the demodulator of this invention are ** explained with reference to drawing 6 etc. Drawing 6 is the block diagram showing one example of the SS modulator 10 of this invention. It sets to this drawing and, for a reference signal generator (oscillator) and 2, the number of multiplying is [1] N1. Frequency multiplier [it is only described as a "multiplier" below], the multiplier for a diffusion modulation in 4, and 5 and 9 — the number of dividing — respectively — N2 and N3 (each of N1, N2, and N3 is the integer of arbitration) — a counting-down circuit — The same sign is given to the same component as equipment 30 conventionally which 7 is LPF, and 8 is a serial juxtaposition (S/P) conversion circuit, in addition was shown in drawing 1 , and the detailed explanation is omitted. In addition, the concrete configuration of the multi-level modulation circuit 3 is as having been shown in drawing 3 .

[0022] Next, concrete actuation of the SS modulator 10 is explained with reference to drawing 6 . Frequency f1 outputted from an oscillator 1 A multiplier 2 and counting-down circuits 5 and 9 are supplied, and a reference signal is N1, respectively. Multiplying and N2 Dividing and N3 After dividing is carried out, the multi-level modulation circuit 3, the diffusion sign generating circuit 6, and the serial juxtaposition (SHIRIPARA) conversion circuit 8 are supplied, respectively.

[0023] thereby — the serial parallel-conversion circuit 8 — setting — input terminal In8 from — a series of information Df1 / N3 a period (conversion timing) — four information signals d1, d2, d3, and d4 the serial parallel conversion is carried out — [— each information — transmission speed [ ] —] which falls to one fourth. Or four information signal d1 -d4 supplied serially It changes into four juxtaposition-signals and outputs to the multi-level modulation circuit 3. And in the multi-level modulation circuit 3, it is the frequency N one f1 from a multiplier 2. It is information signal d1 -d4 by the subcarrier. Multi-level modulation (for example, 16QAM) is carried out, and it is outputting to the multiplier 4.

[0024] On the other hand, in the diffusion sign generating circuit 6, it is f1 from a counting-down circuit 5 / N2. The diffusion sign for a diffusion modulation is generated by making the signal of a frequency into a clock signal, and the multiplier 4 is supplied through LPF7. Therefore, in a multiplier 4, the diffusion modulation of the multi-level modulation wave by multiplication with a diffusion sign is performed, and it is the transmitting antenna A1. It is sent out as an SS modulated wave. In addition, LPF7 may remove components other than the main lobe of a diffusion sign, and there may not not necessarily be. By the way, the period of a diffusion sign (clock signal), the subcarrier for multi-level modulation, and a serial parallel conversion has taken the synchronization so that clearly from the above explanation.

[0025] Next, the SS demodulator 20 is explained with drawing 7 . As shown in this drawing, the SS demodulator 20 of this invention is two or more BPF (band pass filter) 22, 27, and 31, the 46; various amplifier 23, and the 41; mixers (multiplier) 24, 28, and 39 ;P NG (diffusion coder)29, the AGC amplifier 32, counting-down circuits 36, 38, and 44; it has the synchronous detector 33 and parallel-serial (P/S) conversion circuit 43 grade, and these are connected like illustration and it is constituted. In addition, the same sign is given to the same component as equipment 2 conventionally which was shown in drawing 2 in this drawing 7 , and that detailed explanation is omitted. Moreover, the concrete configuration of the multiple-value demodulator circuit 42 is as having been shown in drawing 4 .

[0026] Receiving antenna A2 SS modulated wave which received is supplied to a mixer 24 through BPF22 and the RF amplifier 23. On the other hand, the local oscillation signal outputted from a local oscillator 25 is a frequency by the multiplier 26 N1 Multiplying is carried out, it considers as a multiplying local oscillation signal, and the mixer 24 is supplied. Therefore, frequency conversion of the SS modulated wave is carried out to an intermediate frequency by the mixer 24, and a multiplier 28 is supplied through BPF27.

[0027] On the other hand from the oscillator 35 for synchronous prehension, the signal for synchronous prehension with the frequency near the clock signal frequency for diffusion signs of nonmal is outputted, and this oscillation signal is supplied before SS synchronous establishment to PNG29 through Switch Sw. Therefore, since the diffusion sign for synchronous prehension is outputted from PNG29 and a multiplier 28 is supplied through LPF21, the output of a multiplier 28 turns into a correlation output for SS synchronous prehension. Short SS synchronous point (correlating point) and a comparatively prolonged asynchronous period exist in this correlation output like common knowledge repeatedly in time, and this correlation output is supplied to the multiple-value demodulator circuit 42, the subcarrier regenerative circuit 37, and the synchronous detector 33 through BPF31 and the AGC (automatic gain control) amplifier 32.

[0028] In the decorrelational period of the above-mentioned correlation output, since SS synchronization is not established, a playback subcarrier with many jitters is outputted from the subcarrier regenerative circuit 37, but if it results in a correlating point, the jitter in a playback subcarrier will serve as the minimum. At the correlating point of this short period of time, the playback subcarrier which does not almost have a jitter is N1 dividing. A counting-down circuit 38, a multiplier 39, BPF46, an amplifier 41, and N2 dividing Switch Sw is supplied through a counting-down circuit 36. Since the local oscillation signal from a local oscillator 25 is also supplied to the multiplier 39, it is 1/N1 here. Multiplication with the correlation output by which dividing was carried out is performed. Therefore, from a multiplier 39, two kinds of signals which have the sum of the frequency of both input signals and the frequency of a difference, respectively are outputted. It is the frequency f1 of the reference signal which uses the frequency with said SS modulator 10 like the after-mentioned although only a signal component with a peace (a difference is sufficient) frequency is made to transmit by this example among them BPF46. It becomes the very thing.

[0029] That is, a counting-down circuit 36 is supplied through amplifier 41, and the reference signal which a reference signal playback means is formed and was reproduced by the multiplier 39 and BPF46 here is 1/N2 here. Since dividing is carried out, as for the output, the SS modulator 10 serves as the same a clock signal for diffusion sign generating. On the other hand, if the correlation output supplied to the synchronous detector 33 serves as a correlating point, by detecting for example, threshold level, the synchronous detector 33 will detect it and will output a control signal to Switch Sw. Then, since Switch Sw switches connection to a counting-down circuit 36 side from an oscillator 35, the above-mentioned playback clock signal from a counting-down circuit 36 is supplied to the diffusion coder 29, a diffusion sign equivalent to the diffusion sign in the SS modulator 10 comes to be generated, and SS synchronization is established.

[0030] Moreover, since the jitter of a playback subcarrier serves as the minimum, the recovery actuation in the multiple-value demodulator circuit 42 will also start to SS synchronous establishment and coincidence in an instant, and a multi-level modulation signal restores to it to them in this multiple-value demodulator circuit 42 by the circuitry and the principle of operation which were shown at said drawing 4 , and it is information signal d1 -d4. It is outputted to the parallel-serial-conversion circuit 43 at parallel.

[0031] On the other hand, for the playback reference signal from amplifier 41, the number of dividing is N3. Since the parallel-serial-conversion circuit 43 is supplied as a clock signal through a counting-down circuit 44 [the counting-down circuit 9 of the SS modulator 10, and this function], it is information signal d1 -d4 by parallel-serial (PARASHIRI) conversion. It is changed into the information D on a radical, and is outputted from an output terminal Out6.

[0032] Here, in the SS demodulator 20, drawing 6 drawing 7 is combined, the process in which a playback reference signal is reproduced is referred to, and it explains to ** et al. and a detail the

reference signal frequency from said oscillator 1 — like the above — f1 it is — several multiplying of multipliers 2 and 26 — N1 the carrier frequency which will be supplied to the multi-level modulation circuit 3 if 9 — 9f1 It becomes. Moreover, it is the local oscillation signal frequency from the oscillator 25 in the SS demodulator 20 f2 When it carries out, the multiplying local oscillation signal frequency from a multiplier 26 is 2 9f. It becomes, and the frequency will be set to 9 (f1−f2) if the signal which has the frequency component of a difference among [BPF27] the multiplication outputs from a mixer 24 is made to transmit.

[0033] Therefore, the frequency of the playback subcarrier through BPF31 and amplifier 32 of the subcarrier regenerative circuit 37 is also 9 (f1−f2). On the other hand, for the frequency (fundamental frequency) of the dividing output signal of a counting-down circuit 38, the frequency of the signal which removes a frequency component unnecessary among the multiplication outputs from a multiplier 39 at BPF46, and is acquired since it is (f1−f2) is (f1−f2) +f2 =f1. Since it becomes, it is a frequency f1 from BPF46. It means that the reference signal was reproduced.

[0034] In addition, in this invention, the build up time of the actuation in the SS demodulator 20 is computed as follows. namely, the clock signal frequency for diffusion signs — f1 / N2 it is — if f3 and diffusion code length are set to L for the frequency of the signal for synchronous prehension from an oscillator 1, the synchronous prehension time amount T will become settled in a degree type.

[0035]

T<=L [f1/N2−f3] −1 ..... (1) They are code length L= 31 and f1/N2−f3 =1kHz there. It is T<=31msec if it carries out. It becomes, namely, they are 31msec(s). SS synchronization will be established in a short time called the following. On the other hand, for the subcarrier regenerative circuit 37, since it has started before SS synchronization is established, the sum total of build up time is these 31msec(s). It will fit in less than.

[0036] In the above explanation, although multi-level modulation was made into 16QAM, it is theoretically possible not only this but to make it 64QAM etc., and, naturally the serial parallel conversion of the information D is carried out to eight information signals (d1 −d8) in that case.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the outline block block diagram of the conventional SS modulator.

[Drawing 2] It is the outline block block diagram of the conventional SS demodulator.

[Drawing 3] It is the concrete block block diagram of the multi-level modulation circuit which performs a primary modulation.

[Drawing 4] It is the concrete block block diagram of the multiple-value demodulator circuit which performs a primary recovery.

[Drawing 5] It is the tooth-space diagram (signal point plot plan) of a 16QAM signal.

[Drawing 6] It is the block block diagram of SS modulator of this invention.

[Drawing 7] It is the block block diagram of SS demodulator of this invention.

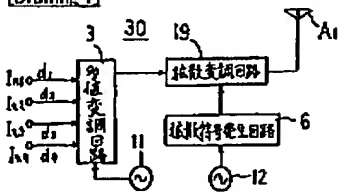
[Description of Notations]

1, 25, 35 Oscillator
2 26 Multiplier
3 Multi-level Modulation Circuit
4 Multiplier (Diffusion Modulation Means)
5, 9, 36, 38, 44 Counting-down circuit
6 29 PNG (diffusion sign generating circuit)
8 Serial Parallel-Conversion Circuit
10 SS Modulator
20 SS Demodulator
22, 27, 31, 46 BPF (band pass filter)
24 Multiplier (Frequency-Conversion Means)
28 Multiplier (Back-Diffusion-of-Electrons Recovery Means)
33 Synchronous Detector
39 Multiplier (Mixer)
43 Parallel-Serial-Conversion Circuit
37 Subcarrier Regenerative Circuit
42 Multiple-Value Demodulator Circuit
A1, A2 Antenna
Sw Circuit changing switch

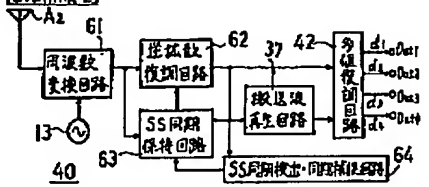
[Translation done.]

DRAWINGS

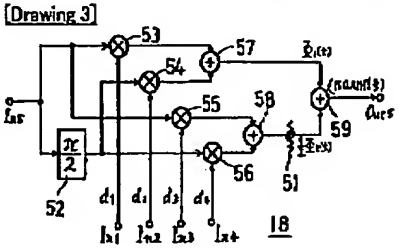
[Drawing 1]



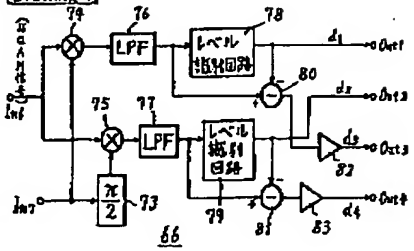
[Drawing 2]



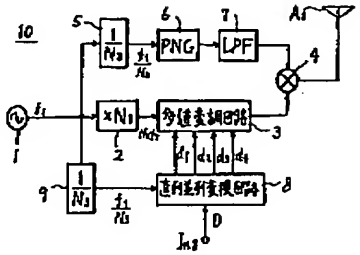
[Drawing 3]



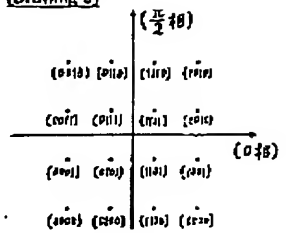
[Drawing 4]



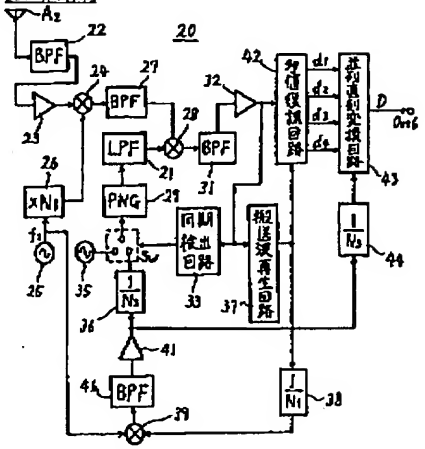
[Drawing 6]



[Drawing 5]



[Drawing 7]



[Translation done.]